# Constantinos Xanthopoulos


Data Scientist

*Dallas, TX*

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## Education

### The University of Texas at Dallas

*Richardson, TX*

Doctor of Philosophy (PhD) in Computer Engineering — *December 2019 (Expected)*

- **Thesis Title:** "Applications of Machine Learning in Test Cost Reduction and Quality Improvement"
- **Advisor:** Dr. Yiorgos Makris
- **Teaching Assistant:** Computer Architecture and Trusted and Secure Integrated Circuits & Systems
- **Research Assistant:** Trusted and RELiable Architectures (TRELA) Lab

Master of Science (MSc) in Computer Engineering — *December 2019 (Expected)*

- **Notable Courses:** Design & Analysis of Computer Algorithms, Statistics for Data Sciences, Cloud Computing, Information Retrieval, Trusted and Secure Integrated Circuits & Systems

### University of Piraeus

*Athens, Greece*

Bachelor of Science (BSc) in Computer Science — *December 2012*

- **GPA:** 8.66/10 (Distinction)
- **Lab Assistant:** Logic Design
- System administrator managing student web & mail server
- Organizing member of the university's open source software student organization

## Industrial Experience

### ams AG

*Graz, Austria*

Machine Learning Engineer (Co-Op) — *Summer 2018*

- Developed a machine learning-based approach for the automation and improvement of the die inking process, currently performed through visual inspection and manual die selection

### Intel Corporation

*Santa Clara, CA*

Data Analyst (Intern) — *Summer 2016*

- Formed the basis of a layout pattern learning framework for systematic defect identification and subsequent automatic test generation. This work contributed in securing a Semiconductor Research Corporation (SRC) grant with the Trusted and RELiable Architectures (TRELA) lab

Data Analyst (Intern) — *Summer 2015*

- Examined the IC defect database through statistical analysis & layout feature extraction and developed a layout template matching tool using existing infrastructure, which automated a previously time-consuming process

### Texas Instruments

*Dallas, TX*

Product Engineer (Co-Op) — *Summer 2014*

- Integrated the trimming cost-reduction methodology in the production flow, demonstrating its practicality & scalability

Product Engineer (Co-Op) — *Summer 2013*

- Researched and developed a novel machine learning-based methodology for adaptive IC trimming, with experimental results showing a 50% reduction in trimming time

## Skills

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| **Industry Knowledge** | Machine Learning, Statistical Modeling, Data Analysis, Data Mining, Data Visualization, Algorithms, Project Management, Web Development, System Administration |
| **Programming Languages** | Python, C, C++, R |
| **Other** | SQL, Unix/Linux Scripting |

# Publications

### Conference Papers

- **C. Xanthopoulos**, K. Huang, A. Poonawala, A. Nahar, B. Orr, J. Carulli, Y. Makris, "IC Laser Trimming Speed-Up through Wafer-level Spatial Correlation Modeling," Proceedings of the IEEE International Test Conference (ITC), 2014
- A. Ahmadi, **C. Xanthopoulos**, A. Nahar, B. Orr, M. Pas, Y. Makris, "Harnessing Process Variations for Optimizing Wafer-Level Probe-Test Flow," Proceedings of the IEEE International Test Conference (ITC), 2016
- **C. Xanthopoulos**, A. Ahmadi, S. Boddikurapati, A. Nahar, B. Orr, Y. Makris, "Wafer-Level Adaptive Trim Seed Forecasting," Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), 2017
- **C. Xanthopoulos**, P. Sarson, H Reiter, Y. Makris, "Automated Die Inking: A Pattern Recognition-Based Approach," Proceedings of the IEEE International Test Conference (ITC), 2017
- G. Rajavendra Reddy, **C. Xanthopoulos**, Y. Makris, "Enhanced Hotspot Detection Through Synthetic Pattern Generation and Design of Experiments," Proceedings of the IEEE VLSI Test Symposium (VTS), 2018
- **C. Xanthopoulos**, D. Neethirajan, S. Boddikurapati, A, Nahar, Y. Makris, "Wafer-Level Adaptive Vmin Calibration Seed Forecasting," Proceedings of the IEEE Design Automation and Test in Europe (DATE), 2019
- D. Neethirajan, **C. Xanthopoulos**, K. Subramani, K. Schaub, I. Leventhal, Y. Makris, "Machine Learning-based Noise Classification and Decomposition in RF Transceivers," IEEE VLSI Test Symposium (VTS), 2019
- **C. Xanthopoulos**, A. Neckermann, P. List, K-P. Tschernay, P. Sarson, Y. Makris, "Automated Die Inking through On-line Machine Learning," IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS), 2019

### Journal Articles

- K. Huang, N. Kupp, **C. Xanthopoulos**, J. M. Carulli Jr., Y. Makris, "Low-Cost Analog/RF IC Testing through Combined Intra- and Inter-Die Correlation Models," Special Issue on Speeding up Analog Integration and Test for Mixed-signal SOCs of the IEEE Design & Test of Computers (D&T), 2015
- G. Rajavendra Reddy, **C. Xanthopoulos**, Y. Makris, "On Improving Hotspot Detection Through Synthetic Pattern-Based Database Enhancement," Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2019 (In Revision)
- **C. Xanthopoulos**, G. Rajavendra Reddy, A. Ahmadi, K. Huang, N. Kupp, J. M. Carulli Jr., Y. Makris, "Wafer-level Spatial Variation Decomposition: An Automated Approach to Process Monitoring," Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2019 (In Review)
- **C. Xanthopoulos**, A. Neckermann, P. List, K-P. Tschernay, P. Sarson, Y. Makris, "Automated Die Inking through On-line Machine Learning," Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2020 (In Preparation)

### Book Chapters

- A. Elfadel, D. Bonning and X. Li (Editors), Machine Learning in VLSI Computer-Aided Design, Springer, 2018 (**C. Xanthopoulos**, K. Huang, A. Ahmadi, N. Kupp, J. Carulli, A. Nahar, B. Orr, M. Pass and Y. Makris, "Gaussian Process-Based Wafer-Level Correlation Modeling and its Applications") (invited)

# References

- Available upon request